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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/700,464	11/15/2000	Terunao Hanaoka	107284	5910

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EXAMINER
ANDUJAR, LEONARDO

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 08/30/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/700,464	HANAOKA ET AL.	
	Examin r	Art Unit	
	Leonardo Andújar	2826	

-- The MAILING DATE of this communication appears on the cov r sheet with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 June 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) *25-36* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *1* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of Group I, claims 1-24 in Paper No. 4 is acknowledged. The traversal is on the ground(s) that the subject matter of claims 1-36 is sufficiently related that a thorough and complete search for the subject matter of the elected claims would necessarily encompass a thorough and complete search for the subject matter of the non-elected claims. Also, the traversal is on the ground that the restriction can only be issued if the asserted groups of claims do not share a common unity of invention. This is not found persuasive because referring to the restriction requirement set forth in the Office Action paper no. 3, it shows that that Group I does not provide a contribution over the prior art since claims 1 and 13 are known in the art as evidenced by US 5,470,787. Therefore, Group I and II do not share any special technical feature. *The expression special technical features is defined as meaning those technical features that define the contribution which each claimed invention, considered as a whole, makes over the prior art.* Additionally, the search is not coextensive as evidenced by the different fields of search for the process and product as cited in the previous restriction requirement. Furthermore, Applicant has not provided a convincing argument that the materially different processes would not be suitable in producing the claimed device. Note that the unpatentability of the Group I invention would not necessarily imply unpatentability of the Group II invention. Thus the requirement is still deemed proper and is therefore made FINAL.

Specification

2. A statement reading "This application is a continuation of PCT application number PCT/JP00/01387 filed on March 08, 2000" should be included on page 1 line 1 of the specification.

Claim Objections

3. Claims 21–24 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claim 21, which recites "a circuit board", does not further limit claim 1, which claims a semiconductor device. Claim 22, which recites "a circuit board", does not further limit claim 13, which claim a semiconductor device. Claim 23, which recites "an electronic instrument", does not further limit claims 1, which claim a semiconductor device. Claim 24, which recites "an electronic instrument", does not further limit claims 13, which claim a semiconductor device.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 3-6, 8-10, 13, 15-18, 21 and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by Greer (US 5,470,787).

6. Regarding claim 1, Greer (e.g. fig. 5) shows a semiconductor device comprising:

- A semiconductor element 24 having a plurality of electrodes 22;
- An interconnect pattern (36, 38, 40) electrically connected to the electrodes;
- And external terminals 42 electrically connected to the interconnect pattern.

7. Also, Greer shows a plurality of insulating layers (26, 28 and 30) formed around the external terminals on the interconnect pattern.

8. Regarding claim 3, Greer shows that the insulating layer 30 can be made of polyimide (col. 8/lls. 25-26).

9. Regarding claim 4, Greer shows that the insulating layers contact the external terminals at opening portions each of which has an inclined surface providing a taper increasing in size form a lower layer to higher layer of the insulating layers.

10. Regarding claim 5, Greer shows that each of the external terminals includes a base and a connection portion provide on the base. Also, the base is provided in an opening portion through which each of the external terminals contact the insulating layers.

11. Regarding claim 6, Greer shows that the insulating layers contact the external terminals at opening portions each of which is formed with a curved surface.

12. Regarding claim 8, Greer shows that the uppermost layer of the insulating layers is formed over the whole surface of the second layer of the insulating layers from the uppermost layer except for an area of the external terminal.

13. Regarding claim 9, Greer shows that the uppermost layer 30 of the insulating layers has an area smaller that an area of the second layer 28 of the insulating layers forms the uppermost layer.

14. Regarding claim 10, Greer shows the insulating layer include an upper layer 30 and a lower layer of different characteristics (i.e. layer thickness).

15. Regarding claim 13, Greer (e.g. fig. 5) shows a semiconductor device comprising:

- A semiconductor element 24 having a plurality of electrodes 22;
- An interconnect pattern (36, 38, 40) electrically connected to the electrodes;
- And external terminals 42 electrically connected to the interconnect pattern.

16. Also, Greer shows that the interconnect pattern is formed on an insulating layer that has protrusions and depressions. The external terminals are formed in the depressions.

17. Regarding 15, Greer shows that the insulating layer is formed of polyimide (col. 8/lls. 25-26).

18. Regarding claim 16, Greer shows that the external terminals includes a base and a connection portion provided on the base. The base and the interconnect pattern are constructed as a single member.

19. Regarding claim 17, Greer shows that the depressions are formed to have an opening extremity lager than the bottom.

20. Regarding claim 18, Greer shows that the insulating layer includes an upper layer 30 and a lower layer 28 of different characteristics (i.e. layer thickness).

21. Regarding claims 21 and 22, Greer that the semiconductor device is mounted in a circuit board (col. 1/lls. 19-29).

Claim Rejections - 35 USC § 103

22. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

23. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

24. Claims 2, 7, 14, 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Greer (US 5,470,787).

25. Regarding claims 2 and 14, Greer shows a plurality of insulating layers. In reference to the claim language referring to stress relieving function, intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the

intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. In re Casey, 152 USPQ 235 (CCPA 1967); In re Otto, 136 USPQ 458, 459 (CCPA 1963).

26. Regarding claim 7, Greer shows that the interconnect pattern is formed on the layer 16 which is below the plurality of insulating layers. In reference to the claim language referring to stress relieving function, intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. In re Casey, 152 USPQ 235 (CCPA 1967); In re Otto, 136 USPQ 458, 459 (CCPA 1963).

27. Regarding claim 23 and 24, Greer discloses that the semiconductor device is mounted on a circuit board (col. 1/lls. 19-29). Official Notice is taken with respect the semiconductor chip is part of an electronic instrument. Thus, to use the semiconductor device disclosed by Greer as a part of an electronic instrument would have been obvious to a person having ordinary skill in the art at the time the invention was made since is very well known in the art that electronic instruments comprises semiconductor chips.

28. Claims 11, 12 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Greer (US 5,470,787) in view of Lehrer (US 4,972,251).

29. Regarding claims 11 and 19, Greer shows most aspects of the instant invention. However, Greer does not disclose the materials of the insulating layers. Therefore, Greer does not disclose that the coefficient of thermal expansion of the upper layer is greater than the coefficient of thermal expansion of the lower layer of the insulating layers. Lehrer (e.g. fig. 3) discloses a semiconductor substrate having a staked passivation layer composed from silicon dioxide-silicon germanium layers 16 and silicon dioxide layer 18 (col. 4/lls. 1-10). Also, Lehrer discloses that the coefficient of thermal expansion of the upper layer 18 is greater than the coefficient of thermal expansion of the lower layer 16 (col. 5/lls. 1-8). This type embodiment enables the semiconductor device to be passivated without the use of high temperature (col. 2/lls. 23-30). It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the insulating layer of Greer from silicon dioxide-silicon germanium layers and silicon dioxide layer in order to passivate the device without the use of high temperature as suggested by Lehrer. Note: It is implicit that the coefficient of thermal expansion of the upper layer will be greater than the coefficient of thermal expansion of the lower layer of the insulating layer.

30. Regarding claims 12, Greer shows most aspects of the instant invention. However, Greer does not disclose the materials of the insulating layers. Therefore, Greer does not disclose that the Yong's modulus of the lower layer is greater than the Young's modulus of the upper layer of the insulating layers. Lehrer (e.g. fig. 3) discloses a semiconductor substrate having a staked passivation layer composed from silicon dioxide-silicon germanium layers 16 and silicon dioxide layer 18 (col. 4/lls. 1-10). Also,

Lehrer discloses that the Yong's modulus of the lower layer 16 is greater than the Young's modulus of the upper layer 18 (col. 4/lls. 25-33). This type embodiment enables the semiconductor device to be passivated without the use of high temperature (col. 2/lls. 23-30). It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the insulating layer of Greer from silicon dioxide-silicon germanium layers and silicon dioxide layer in order to passivate the device without the use of high temperature as suggested by Lehrer. Note: It is implicit that the Yong's modulus of the lower layer will be greater than the Young's modulus of the upper layer of the insulating layer.

31. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Greer (US 5,470,787) in view of Kitayama et al. (US 5744382).

32. Regarding claim 20, Greer shows most aspects of the instant invention (see comments above). However, Greer does not disclose a protective film formed on the uppermost layer of the semiconductor device. Kitayama (e.g. fig. 7) shows a semiconductor device having a protective film 4 formed on its uppermost layer. Also, Kitayama discloses that the protective layer is used to protect the device electronic components against oxidation and moisture (col. 4/lls. 3-8). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a protective film on the upper most layer of the semiconductor device disclosed by Greer to protect its electronic components against oxidation and moisture as suggested by Kitayama.

Conclusion

33. Papers related to this application may be submitted directly to Art Unit 2826 by facsimile transmission. Papers should be faxed to Art Unit 2826 via the Art Unit 2826 Fax Center located in Crystal Plaza 4, room 3C23. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2826 Fax Center number is **(703) 308-7722** or **–7724**. The Art Unit 2826 Fax Center is to be used only for papers related to Art Unit 2826 applications.

34. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Leonardo Andújar** at **(703) 308-0080** and between the hours of 9:00 AM to 6:00 PM (Eastern Standard Time) Monday through Friday (with alternated Fridays off) or by e-mail via Leonardo.Andujar@uspto.gov. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn, can be reached on (703) 308-6601.

35. Any inquiry of a general nature or relating to the status of this application should be directed to the **Group 2800 Receptionist** at **(703) 305-3900.**

36. The following list is the Examiner's field of search for the present Office Action:

Field of Search	Date
U.S. Class / Subclass (es): 257/692 and 438/108	08/02
Other Documentation:	
Electronic Database(s): East (USPAT, US PGPUB, JPO, EPO, Derwent, IBM TDB)	08/02

Leonardo Andújar
Patent Examiner Art Unit 2826
LA
8/20/02